ENGINEERING
DataXpress

DXL1500 Verilog® Netlist Translator

The DXL1500 netlist translator is one of a series of optimized data links that is part of the DataXpress Integrator™ product line. The DataXpress Integrator ensures complete data interoperability between the various EDA vendors which are supported by the product line.

The DXL1500 netlist translator allows Verilog users to translate their circuit descriptions to and from the Engineering DataXpress database called EDI. Data from the EDI database can be output as an EDIF data file. EDIF netlist files can also be read into the EDI database and translated into the Verilog format.

The DXL1500 can also be combined with other Engineering DataXpress translators to facilitate direct database translation between Verilog and the EDA vendors that are currently supported.

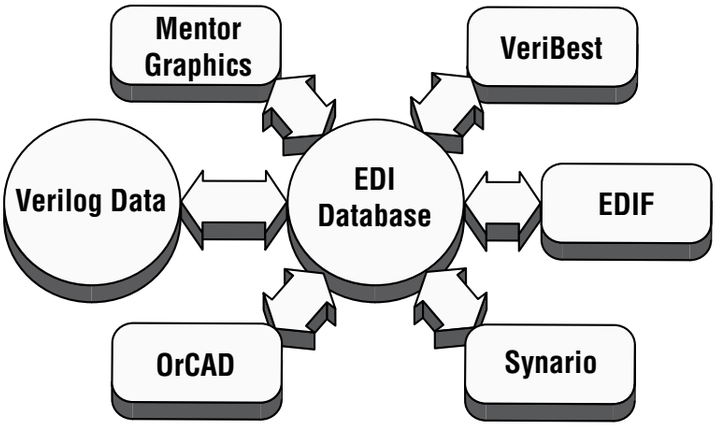
The DXL1500 accepts a complete Verilog structural description as input and generates an EDIF description and a log file. Any behavioral constructs in the Verilog description are ignored. The translator also accepts EDIF 2 0 0 netlist files and converts them into Verilog descriptions.

The DXL1500 uses command line options and configuration files to provide the user with control over how the translator functions. Command line options are used to give the translator the basic input and output information it needs to run.

The DXL1500 netlist translator is fully supported by Engineering DataXpress, a worldwide leader in data integration technology. This ensures that the translator will continue to be enhanced with new features and options. It will also remain current with each new release of Verilog software.

Features

- Translation of structural Verilog to and from EDIF 2 0 0.
- User-controlled generation of EDIF array and bundle representation of Verilog vector nets, bit selects, and port list concatenations.
- Flexible handling of the Verilog built-in gates and switches, which may be represented in other design capture systems and languages.
- User-controlled generation and use of Verilog parameters and specparams to represent EDIF properties.
- Flexible name conversion in EDIF, before translation to Verilog, or after translation from Verilog.



DataXpress Integrator™

Product Description

The DXL1500 translator is a bidirectional netlist translator for transferring Verilog descriptions between various EDA vendors. All Verilog information passes through the DataXpress EDI database. It can then be transferred to and from other EDA vendors who are also linked to the EDI database or to any EDA vendor that has an EDIF netlist interface.

The DXL1500 translator is comprised of two modules. The ver2edi module takes as its input a structural Verilog netlist file and creates as its output either an EDI database or an EDIF file and a log file. The log file contains a run-time transcript of the ver2edi informatory, warning and error messages. All Verilog identifiers are preserved in the EDIF file using the rename form and appropriate EDIF names are generated for these.

All of the Verilog predefined primitives are mapped into an external library. All module and UDP definitions are mapped into one or more EDIF library constructs (design libraries). The mapping of different cells into these libraries can be specified by the user. In addition, other Verilog constructs such as vector ports and concatenations in port definitions, parameters, specparams, path delays, defparams, drive strength, nets/wires, net delay, etc., are mapped to their equivalent EDIF representations.

The edi2ver module takes as its input an EDIF 2 0 0 file and creates Verilog files and libraries. The EDIF file is checked according to EDIF's syntactic and semantic restrictions. Command line options and configuration files provide the user with control over the translation process.

The ver2edi and edi2ver modules use command line options and configuration files to provide the user with control over the translation process. The following are some of the user options which can be specified:

- The location of the Verilog file and the configuration file.
- The locations where the log file and the generated EDIF output should be placed.
- The grouping of cells into EDIF libraries.
- The scaling of delay values.
- The property names for representing net type and charge strength.

Supported Platforms

- PC Windows 95/98 or NT.
- Sun4/SunOS 4.1.4+
- Sun4/SunOS 5.x (Solaris 2.x).
- HP9000/7xx HP-UX 9.xx or greater.

Integrating Engineering Data

ENGINEERING DataXpress

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